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Page 1 of 21
Date: 28-Feb-06

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United States Patent and Trademark Office
Mail Stop Appeal Brief - Patents

From: Cynthia Thomas Faatz **Fax:** 408-765-4087 **Phone:** 503-268-7347

Subject: **Appeal Brief In Application Serial No. 10/816,018**

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Application No.: 10/816,018
Filing Date: March 31, 2004
First Named Inventor: Marijan Persun et al.
Group Art Unit: 2829
Examiner Name: Nguyen, Tung X.
Attorney Docket No.: 42P14976X

Enclosures:
1. Transmittal Form (1 page).
2. Fee Transmittal for FY 2006 (1 page in duplicate).
3. Appeal Brief (17 pages).

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	20

Application Number	10/818,018
Filing Date	March 31, 2004
First Named Inventor	Marijan Persun et al.
Art Unit	2829
Examiner Name	Nguyen, Tung X.
Attorney Docket Number	42P14976X

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
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  - [ ] Affidavits/declaration(s)
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- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
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- [ ] Drawing(s)
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- [ ] Petition to Convert to a Provisional Application
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- [ ] After Allowance Communication to TC
- [✓] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Corporation		
Signature	/Cynthia Thomas Faatz/		
Printed name	Cynthia Thomas Faatz		
Date	February 28, 2006	Reg. No.	39,973

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FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/816,018
Filing Date	March 31, 2004
First Named Inventor	Marlan Persun et al.
Examiner Name	Nguyen, Tung X.
Art Unit	2829
Attorney Docket No.	42P14976X

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	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	0
Design	200	100	100	50	130	65	0
Plant	200	100	300	150	160	80	0
Reissue	300	150	500	250	600	300	0
Provisional	200	100	0	0	0	0	0

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
26 - 20 or HP =	0	x 50	= 0

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
3 - 3 or HP =	0	x 200	= 0

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
360	0

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If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
0 - 100 =	0	/ 50 = 0 (round up to a whole number)	x 0	= 0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	0
Other (e.g., late filing surcharge): Appeal Brief Under 37 C.F.R. section 41.37	500.00

SUBMITTED BY

Signature	/Cynthia Thomas Faatz/	Registration No. (Attorney/Agent) 39,973	Telephone 530-268-7347
Name (Prin/Type)	Cynthia Thomas Faatz		Date February 28, 2006

42P14976X *Patent*

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:		
Marijan Peršun et al.	Examiner:	Nguyen, Tung X.
Serial No.: 10/816,018	Art Unit:	2829
Filing Date: March 31, 2004		
For: A METHOD AND APPARATUS FOR MEASURING RELATIVE, WITHIN DIE LEAKAGE CURRENT AND/OR PROVIDING A TEMPERATURE VARIATION PROFILE USING A LEAKAGE INVERTER AND RING OSCILLATOR		

Mail-Stop Appeal Brief - Patents
Commissioner for Patents
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Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Appellants submit herewith an Appeal Brief as required by 37 C.F.R. § 41.37. This Appeal Brief is in response to the Final Office Action dated September 29, 2005 and the Advisory Action dated December 13, 2005.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, a corporation of Delaware.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants which relate to, directly affect or are directly affected by the Board's decision in this appeal.

III. STATUS OF THE CLAIMS:

Claims 1-28 are pending in this application.

Claims 1-7 stand finally rejected under 35 U.S.C. § 102(b) as considered to be anticipated by U.S. Patent No. 5,410,278 to Itoh et al. ("Itoh").

Claims 8-12 stand finally rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Itoh in view of U.S. Patent No. 6,657,504 to Deal et al. ("Deal").

Claims 26-28 stand finally rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Deal in view of Itoh.

Claims 13-25 are allowed.

The rejections of claims 1-12 and 26-28 are appealed. These claims are reproduced in the attached Claims Appendix, which includes all currently pending claims.

IV. STATUS OF AMENDMENTS:

An After Final Amendment was filed on November 29, 2005. In the After Final Amendment, claims 1, 7 and 26 were amended to more particularly point out and distinctly claim the subject matter that appellants regard as the invention

to place the claims in better form for consideration on appeal. The Advisory Action mailed December 13, 2005 indicates at item 7 that the After Final Amendment will be entered for purposes of appeal.

A copy of the claims on appeal (claims 1-12 and 26-28) is provided in the attached Claims Appendix, which includes all currently pending claims.

V. SUMMARY OF THE INVENTION:

Regarding independent claims 1, 7 and 26 an apparatus or method may include a circuit element (e.g. an inverter or other arrangement of n-type and p-type devices) having a switching delay in only one direction that is directly proportional to a leakage current of one of the devices in the circuit element (page 5, para. [0015] – page 12, para. [0036], Figures 1A (element 100), 1B (element 150), 2A-2D (elements 200, 250, 270 and 280, respectively)). The circuit element of the apparatus or method may be included in one or more ring oscillators (page 12, para. [0037] – page 23, para. [0069], Figures 3-8 (elements 300, 400, 500, 600, 700 and 800, respectively), Figures 10-11 and 13-14), which may include an enable input (page 15. para. [0045] – page 16, para. [0048], e.g. Figure 3, element 325) to control enablement of the one or more ring oscillators and/or control at least a first leakage inverter. The frequency of the one or more ring oscillators may be used to determine one of a local temperature or relative leakage current (e.g. page 23, para. [0070] – page 25, para. [0076], Figure 12, acts 1225 and 1230).

VI. GROUNDS OF REJECTION:

A. Claims 1-7 stand finally rejected under 35 U.S.C. § 102(b) as considered to be anticipated by U.S. Patent No. 5,410,278 to Itoh et al. ("Itoh").

B. Claims 8-12 stand finally rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Itoh in view of U.S. Patent No. 6,657,504 to Deal et al. ("Deal").

C. Claims 26-28 stand finally rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Deal in view of Itoh.

VII. ARGUMENT:

A. Claims 1-7 are patentable under 35 U.S.C. § 102(b) over Itoh

Appellants respectfully traverse the 35 U.S.C. § 102(b) rejection of claims 1-7 over Itoh.

Claim 1 includes the limitations

> an n-type and a p-type device coupled between first and second supply voltages at a terminal; and
> an output node coupled to the terminal, the output node, during operation of the apparatus, to provide an output signal having a switching delay in only one direction that is directly proportional to a leakage current of one of the n-type and p-type devices.

(Claim 1)(Emphasis added).

Appellants respectfully submit that Itoh fails to teach at least the claimed apparatus as set forth in claim 1 to provide an inverted output signal having a transition delay in only one direction that is proportional to a leakage current of a device of the apparatus.

Itoh discloses a ring oscillator that includes a plurality of inverters (11a, 11b and 11c in Figure 1), a leakage current generating part (12), and a current controlling part (13). The current controlling part supplies the inverters with a source current in accordance with a value of a leakage current generated from the leakage current generating part. The leakage current generated from the leakage current generating part is correlated with a leakage current generated from a memory cell. (Itoh, Abstract).

Figure 3a of Itoh shows the inverter circuits of Itoh in more detail and Figure 3b shows the relationship between the input voltage "A" and the output voltage B of the inverter 11a. There is no disclosure in Itoh to teach or suggest that a transition in only one direction at an output node is correlated with a leakage current of a device in the apparatus of Itoh.

In the Final Office Action, it is stated that the Examiner disagrees with Appellants' position as stated above because it appears that the leakage current generated from the memory cell would inherently include a leakage current of the inverter itself. (Final Office Action mailed September 29, 2005, page 7, paragraph 8). In the Advisory Action, it is stated that Itoh teaches in Fig. 1, 11a-c in a ring oscillator having inverters in series together, and the signal of each one having transition in only one direction (figure 1) and that is proportional to a leakage current of a device of an inverter (12 of figure 1).

Assuming, for purposes of argument, that the leakage current generated from the memory cell of Itoh would inherently include a leakage current of an inverter of Itoh, Itoh would still fail to teach or suggest the claimed output node

that has a transition in only one direction that is proportional to a leakage current of a device of an inverter.

The Examiner appears to be stating that each of the inverters in the ring oscillator has a signal that transitions in just one direction, and that that transition is proportional to a leakage current of a device of the inverter. This, however, is not a fair characterization of the claims.

As is well-known in the art, observance of a signal output from an inverter indicates transitions from high to low and from low to high over time, i.e. transitions in both directions. As set forth in claim 1, the claimed apparatus has a switching delay in only one direction that is proportional to a leakage current of a device in the apparatus.

Because the Office Action does not provide any evidence that Itoh includes such a limitation, a *prima facie* case of anticipation has not been established.

For at least this reason, claim 1 is patentably distinguished over Itoh. Claims 2-5 depend from and further limit claim 1, and thus, should also be found to be patentably distinguished over Itoh for at least the reasons set forth above.

Hence, the § 102(b) rejection of claims 1-7 is improper and should be reversed.

B. Claims 8-12 are patentably distinguished under 35 U.S.C. § 103(a) over Itoh and Deal, alone or in combination

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See e.g. M.P.E.P. § 2143.

Appellants respectfully traverse the § 103(a) rejection of claims 8-12 over Itoh in view of Deal. A *prima facie* case of obviousness has not been established at least because there is no motivation to combine the references and, even if they were to be combined, the combination would fail to teach or suggest the claimed features of appellants' invention.

It is stated in the Final Office Action that a combination of Itoh and Deal teaches the claimed features of applicants' invention as set forth in claims 8-12. Appellants respectfully submit that such a combination would not be made.

In particular, Itoh determines the oscillating frequency of a ring oscillator based on a leakage current of a leakage generating part (as argued above) while Deal determines the oscillating frequency of a ring oscillator based on a ring clock count value and a system clock count value (Deal, Abstract). Thus, one of ordinary skill in the art would not have been motivated to combine Itoh and Deal.

Further, even if Deal and Itoh were to be combined, the combination would still fail to teach or suggest the claimed features of appellants' invention.

Claims 8-12 depend from and further limit claim 7, which includes a similar limitation as claim 1 argued above.

For at least the reasons argued above in reference to claim 1, Itoh does not teach or suggest the claimed features of appellants' invention including at least the claimed apparatus that provides an output signal having transition delay in only one direction that is proportional to a leakage current of one of a p- and an n-type device in the apparatus.

Further, there is no teaching or suggestion in Deal, and the Examiner does not suggest that there is any teaching in Deal, of the claimed apparatus that provides an output signal having a transition delay that is related to leakage, much less a transition delay in only one direction that is proportional to a leakage current of one of a p or n type device in the apparatus. Thus, the combination of Itoh and Deal would also fail to teach or suggest such a feature.

For at least this reason, claims 8-12, which depend from and further limit claim 7, are patentably distinguished over Itoh and Deal, alone or in combination. The rejection under 35 U.S.C. § 103(a) of claims 8-12 is therefore improper and should be withdrawn.

C. Claims 26-28 are patentably distinguished under 35 U.S.C. § 103(a) over Deal and Itoh, alone or in combination

Appellants respectfully traverse the § 103(a) rejection of claims 26-28 over Deal in view of Itoh.

First, as argued above in reference to claims 8-12, there is no motivation to combine the Deal and Itoh references.

Second, even if such a combination were to be made, the combination would still fail to teach or suggest the claimed features of appellants' invention.

Independent claim 26, like independent claim 7, sets forth a leakage inverter and includes a limitation similar to that argued above in reference to claim 1. For at least the same reasons argued in reference to claim 1 and claims 8-12 (and claim 7 implicitly), a combination of Deal and Itoh, were such a combination to be made, would fail to teach or suggest the claimed features of applicants' invention as set forth in claim 26 including at least detecting a frequency of a leakage ring oscillator on an integrated circuit wherein the leakage ring oscillator includes at least a first leakage inverter to provide an inverted output signal having a transition delay in only one direction that is proportional to a leakage current of a device of the leakage inverter over a first temperature range.

Claims 27-28 depend from and further limit claim 26.

Thus, claims 26-28 should be found to be patentably distinguished over Deal and Itoh, alone or in combination.

The rejection of claims 26-28 under 35 U.S.C. § 103(a) is therefore improper and should be withdrawn.

CONCLUSION

For the reasons set forth above, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejection of claims 1-12 and 26-28.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

Dated: February 28, 2006 /Cynthia Thomas Faatz/

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CERTIFICATE OF TRANSMISSION

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Cynthia Thomas Faatz
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/Cynthia Thomas Faatz/
Signature

Claims Appendix

1. (Currently Amended) An apparatus comprising:

an n-type and a p-type device coupled between first and second supply voltages at a terminal; and

an output node coupled to the terminal, the output node, during operation of the apparatus, to provide an output signal having a switching delay in only one direction that is directly proportional to [[the]] a leakage current of one of the n-type and p-type devices.

2. (Original) The apparatus of claim 1 wherein

the n-type and p-type devices are coupled to function as an inverter.

3. (Original) The apparatus of claim 1 wherein

drains of the n-type and p-type devices are coupled to each other at the terminal;

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal, and

a gate of a second one of the n-type and p-type devices is coupled to receive a bias voltage during operation that results in the gate-to-source voltage of the second device being less than the threshold voltage of the second device.

4. (Original) The apparatus of claim 3 wherein the gate of the second device is coupled to the source of the second device.

5. (Original) The apparatus of claim 1 wherein

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal, and

a gate of a second one of the n-type and p-type devices is coupled to the output node and the source and drain of the second one of the n-type and p-type devices are both coupled to receive one of the first and second supply voltages.

6. (Original) The apparatus of claim 1 wherein

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal,

a gate of a second one of the n-type and p-type devices is coupled to receive one of the first and second supply voltages, and

a source and drain of the second device are both coupled to the output node.

7. (Currently Amended) An apparatus comprising:

a ring oscillator including,

at least one leakage inverter to provide an inverted output signal having a signal transition delay in only one direction that is proportional to a leakage current of a device of the first leakage inverter, and

one or more static stages,

the ring oscillator to provide an oscillating output signal.

8. (Original) The apparatus of claim 7 wherein

the at least one leakage inverter includes a leaky device having a gate coupled to a receive a bias voltage during operation, the bias voltage being a sub-threshold gate-to-source voltage, and

wherein the leakage current is a drain leakage current.

9. (Original) The apparatus of claim 8 wherein

the gate of the leaky device is coupled to receive an enable signal, the leaky device to be turned on in response to the enable signal being deasserted.

10. (Original) The apparatus of claim 7 wherein,

the at least one leakage inverter includes a leaky device having a source and drain coupled to receive a supply voltage and a gate coupled to an output node of the leakage inverter, and

wherein the leakage current is a gate leakage current.

11. (Original) The apparatus of claim 7 wherein,

the at least one leakage inverter includes a leaky device having a gate coupled to receive a supply voltage and a source and drain coupled to an output node of the leakage inverter.

12. (Original) The apparatus of claim 7 wherein,

the ring oscillator includes at least three leakage inverters, and

wherein a frequency of the oscillating output signal varies in proportion to the leakage current of the device.

13. (Original) An apparatus comprising:

an enable input to receive an enable signal; and

a leakage ring oscillator to be enabled in response to the enable signal being asserted, the leakage ring oscillator including

at least a first leakage inverter including a leaky device, the leaky device to be substantially fully turned on in response to the enable signal being deasserted; and

an output to provide an oscillating output signal in response to the leakage ring oscillator being enabled, a frequency of the oscillating output signal being dependent upon a leakage current of the first leakage inverter while the leakage ring oscillator is enabled.

14. (Original) The apparatus of claim 13 wherein the leakage ring oscillator includes at least three leakage inverters, each of the three leakage inverters including a leaky device to be substantially fully turned on and another device to be substantially fully turned off in response to the enable signal being deasserted.

15. (Original) The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device coupled to receive a sub-threshold gate-to-source voltage in response to the enable signal being asserted.

16. (Original) The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device having a source and drain coupled to receive a same supply voltage and a gate coupled to an output of the leakage inverter.

17. (Original) The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device having a gate coupled to receive a supply voltage and a source and drain both coupled to an output of the leakage inverter.

18. (Original) The apparatus of claim 14 wherein at least one of the three leakage inverters is coupled such that the leakage current is a drain leakage current.

19. (Original) The apparatus of claim 14 wherein at least one of the three leakage inverters is coupled such that the leakage current is a gate leakage current.

20. (Original) An integrated circuit comprising:

a plurality of leakage ring oscillators, each of the leakage ring oscillators including at least a first leakage inverter to provide an inverted output signal having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter, each of the plurality of leakage ring oscillators to provide an oscillating output signal, a frequency of the respective oscillating output signal to indicate at least one of a local temperature and leakage current; and

an externally-accessible output circuit coupled to receive the oscillating output signal.

21. (Original) The integrated circuit of claim 20 wherein the externally-accessible output circuit is a test access port.

22. (Original) The integrated circuit of claim 20 wherein the externally-accessible output circuit includes a control register.

23. (Original) The integrated circuit of claim 20 wherein

at least one of the leakage ring oscillators includes at least three leakage inverters.

24. (Original) The integrated circuit of claim 23 wherein the at least three leakage inverters indicate local gate leakage.

25. (Original) The integrated circuit of claim 23 wherein the at least three leakage inverters indicate local channel leakage.

26. (Currently Amended) A method comprising:

detecting a frequency of a leakage ring oscillator on an integrated circuit, the leakage ring oscillator including at least a first leakage inverter to provide an inverted output signal having a transition delay in only one direction that is proportional to a leakage current of a device of the leakage inverter over a first temperature range; and

determining one of a local temperature or relative leakage current in response to the detected frequency.

27. (Original) The method of claim 26 wherein determining comprises

accessing data indicating leakage ring oscillator frequency versus at least one of temperature and leakage current.

28. (Original) The method of claim 26 further comprising:

characterizing each of the leakage ring oscillators at different temperatures; and

developing a look-up table indicating frequency of the oscillating output signal versus temperature.